In re Patent Application of:
STORM ET AL.
Serial No. **10/820,464**
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In the Specification:

Please replace paragraph 19 beginning at page 4 with the following rewritten paragraph:

[0019] For linear operation the reset voltage Vrt (set in col4) can be sampled onto the node pix by pulsing cal/reset high (applied to transistor M4) and logsel (applied to transistor M6) can be raised to precharge the gate of transistor M2 via col3 low such that it is off and does not affect the integration period. If isolate (applied to transistor M5) is on then the photocurrent generated will lower the voltage on pix. After a set integration time read can be turned on such that M1 now acts as a source follower, with column 2 held at a voltage approximately equal to the reset voltage Vrt and column 1 comprising a current source (not shown).